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EXAMINER	
MOORE JR, MICHAEL J	

ART UNIT	PAPER NUMBER
2419	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/603,792	MAUFER ET AL.	
	Examiner	Art Unit	
	MICHAEL J. MOORE, JR.	2419	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _28 October 2008_.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _3-17 and 23-27_ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _3-17 and 23-27_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 11/19/08 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Objections

1. Claim **11** is objected to because of the following informalities: On line 13, the word “the” before the word “predetermined” should be “a” in this first instance of the claimed “predetermined time”.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims **3, 4, 11, 12, 23, and 24** are rejected under 35 U.S.C. 103(a) as being unpatentable over Bilic et al. (U.S. 7,050,437) (hereinafter “Bilic”) in view of Malagrino et al. (U.S. 6,714,985) (hereinafter “Malagrino”).

Regarding claim **3**, *Bilic* teaches the frame reassembly method via network interface adapter 20 shown in Figure 2.

Bilic also teaches the reception of a detected fragment of a frame as spoken of on column 7, lines 48-51.

Bilic also teaches the IP header checksum computation of the frame reassembled from received fragments as spoken of on column 8, lines 48-52.

Bilic also teaches the allocation of space in host memory 44 (buffer space) for received fragments of a frame as spoken of on column 8, lines 1-6.

Bilic also teaches the processor 34 setting a frame timer for the frame as spoken of on column 8, lines 8-9.

Bilic also teaches the processor (network interface circuitry) that organizes (sorting) the fragments in the host memory (buffer space) based on the fragment offset fields (fragment number) and length parameters in the fragment headers as spoken of on column 3, lines 23-25 as well as column 8, lines 31-34.

Bilic also teaches the processor (network interface circuitry) that periodically determines that one or more fragments have been lost (missing) in the event that a given frame has not been reassembled completely within a predetermined time limit as spoken of on column 3, lines 30-33 as well as column 8, lines 14-19.

While *Bilic* also teaches the reassembly of packet fragments by network interface adapter 20 and forwarding (transmission) of the reassembled packet data to a host 24 via a bus interface 40 and host bus 42, *Bilic* does not explicitly teach "transmitting the first packet from the network interface circuitry <u>over a network</u> to a receiver".

However, *Malagrino* teaches a system and method for efficient reassembly of fragments, where upon a switch S5 receiving fragments 212 of a packet, switch S5 reassembles the fragments into packet 210 and subsequently forwards the packet 210 <u>over network 230</u> to host H2 (receiver) as shown in Figure 2 and spoken of on column 6, lines 1-11.

At the time of the invention, it would have been obvious to someone of ordinary skill in the art, given these references, to apply the above reassembled packet transmission teachings of *Malagrino* to the teachings of *Bilic* in order to provide support for packet forwarding to hosts that are located remotely from the packet fragment reassembly processor as spoken of on column 6, lines 1-11 of *Malagrino*.

Regarding claim **4**, *Bilic* further teaches the processor 34 instructing logic 36 to free (clearing) the buffer space reserved for a frame having lost fragments as spoken of on column 8, lines 19-22.

Regarding claim **11**, *Bilic* teaches the frame reassembly method shown in Figure 2 performed by the header processor 34 (network interface) coupled to fast memory 32 (computer readable medium) as shown in Figure 1.

Bilic also teaches the reception of a detected fragment of a frame as spoken of on column 7, lines 48-51.

Bilic also teaches the IP header checksum computation of the frame reassembled from received fragments as spoken of on column 8, lines 48-52.

Bilic also teaches the allocation of space in host memory 44 (buffer space) for received fragments of a frame as spoken of on column 8, lines 1-6.

Bilic also teaches the processor 34 setting a frame timer for the frame (relative to first packet) as spoken of on column 8, lines 8-9.

Bilic also teaches the processor (network interface circuitry) that organizes (sorting) the fragments in the host memory (buffer space) based on the fragment offset fields (fragment number) and length parameters in the fragment headers as spoken of on column 3, lines 23-25 as well as column 8, lines 31-34.

Bilic also teaches the processor (network interface circuitry) that periodically determines that one or more fragments have been lost (missing) in the event that a given frame has not been reassembled completely within a predetermined time limit as spoken of on column 3, lines 30-33 as well as column 8, lines 14-19.

While *Bilic* also teaches the reassembly of packet fragments by network interface adapter 20 and forwarding (transmission) of the reassembled packet data to a host 24 via a bus interface 40 and host bus 42, *Bilic* does not explicitly teach "transmitting the first packet from the network interface circuitry <u>over a network</u> to a receiver".

However, *Malagrino* teaches a system and method for efficient reassembly of fragments, where upon a switch S5 receiving fragments 212 of a packet, switch S5 reassembles the fragments into packet 210 and subsequently forwards the packet 210

over network 230 to host H2 (receiver) as shown in Figure 2 and spoken of on column 6, lines 1-11.

At the time of the invention, it would have been obvious to someone of ordinary skill in the art, given these references, to apply the above reassembled packet transmission teachings of *Malagrino* to the teachings of *Bilic* in order to provide support for packet forwarding to hosts that are located remotely from the packet fragment reassembly processor as spoken of on column 6, lines 1-11 of *Malagrino*.

Regarding claim **12,** *Bilic* further teaches the processor 34 instructing logic 36 to free (clearing) the buffer space reserved for a frame having lost fragments as spoken of on column 8, lines 19-22.

Regarding claim **23**, *Bilic* teaches the network interface adapter 20 (system) of Figure 1 that performs the frame reassembly method shown in Figure 2.

Bilic also teaches the CPU 46 shown in Figure 1.

Bilic also teaches the host memory 44 shown in Figure 1.

Bilic also teaches the header processor 34 (network interface) shown in Figure 1.

Bilic also teaches the reception of a detected fragment of a frame as spoken of on column 7, lines 48-51.

Bilic also teaches the IP header checksum computation of the frame reassembled from received fragments as spoken of on column 8, lines 48-52.

Bilic also teaches the allocation of space in host memory 44 (buffer space) for received fragments of a frame as spoken of on column 8, lines 1-6.

Bilic also teaches the processor 34 setting a frame timer for the frame (relative to first packet) as spoken of on column 8, lines 8-9.

Bilic also teaches the processor (network interface) that organizes (sorting) the fragments in the host memory (buffer space) based on the fragment offset fields (fragment number) and length parameters in the fragment headers as spoken of on column 3, lines 23-25 as well as column 8, lines 31-34.

Bilic also teaches the processor (network interface) that periodically determines that one or more fragments have been lost (missing) in the event that a given frame has not been reassembled completely within a predetermined time limit as spoken of on column 3, lines 30-33 as well as column 8, lines 14-19.

While *Bilic* also teaches the reassembly of packet fragments by network interface adapter 20 and forwarding (transmission) of the reassembled packet data to a host 24 via a bus interface 40 and host bus 42, *Bilic* does not explicitly teach "transmitting the first packet from the network interface circuitry over a network to a receiver".

However, *Malagrino* teaches a system and method for efficient reassembly of fragments, where upon a switch S5 receiving fragments 212 of a packet, switch S5 reassembles the fragments into packet 210 and subsequently forwards the packet 210 over network 230 to host H2 (receiver) as shown in Figure 2 and spoken of on column 6, lines 1-11.

At the time of the invention, it would have been obvious to someone of ordinary skill in the art, given these references, to apply the above reassembled packet transmission teachings of *Malagrino* to the teachings of *Bilic* in order to provide support

for packet forwarding to hosts that are located remotely from the packet fragment reassembly processor as spoken of on column 6, lines 1-11 of *Malagrino*.

Regarding claim **24**, *Bilic* further teaches the header processor 34 instructing logic 36 to free (clearing) the buffer space reserved for a frame having lost fragments as spoken of on column 8, lines 19-22.

5. Claims **5-10, 13-17, and 25-27** are rejected under 35 U.S.C. 103(a) as being unpatentable over Bilic et al. (U.S. 7,050,437) (hereinafter "Bilic") in view of Malagrino et al. (U.S. 6,714,985) (hereinafter "Malagrino") in view of Robotham et al. (U.S. 6,775,293) (hereinafter "Robotham") and in further view of Natanson et al. (U.S. 6,611,525) (hereinafter "Natanson").

Regarding claims **5, 13, and 25,** *Bilic* in view of *Malagrino* teaches the limitations as described above. *Bilic* further teaches the frame reassembly completion and storage in host memory 44 (memory) spoken of on column 8, lines 48-57.

Bilic in view of *Malagrino* does not teach "incrementing a counter of the network interface circuitry; checking a connection table entry for the first packet; responsive to non-existence of the connection table entry, sending the first packet to network interface software for preparing the first packet for the network interface circuitry; generate an address resolution table (ART) index for an address resolution table entry that stores a media access control (MAC) address and MAC layer attributes, build the connection table entry, including the ART index, at least partially process the first packet, and send the first packet as processed to the network interface circuitry; forwarding the first

packet from the network interface circuitry; clearing the buffer of the first packet responsive to forwarding the first packet; and decrementing the counter”.

However, *Robotham* teaches the incrementing of count values of count table 40 (counter) as received data units (packets) are stored in the buffer 20 as spoken of on column 2, lines 45-48.

Robotham also teaches the referencing (checking) of a context table (connection table) upon reception of data units (packets) as spoken of on column 2, lines 43-45.

Robotham also teaches transmission block 50 that determines stream identifiers (packet processing) corresponding to fetched data units (packets) as spoken of on column 3, lines 45-49.

Robotham also teaches transmission block 50 that transmits (forwards) the fetched data units (packets) as transmitted data units as spoken of on column 3, lines 56-58.

Robotham also teaches the dequeuing of data from the buffer (clearing the buffer) for forwarding as spoken of on column 2, lines 49-50.

Robotham also teaches the decrementing of count values of count table 40 (counter) as data units are retrieved from the buffer and transmitted as spoken of on column 3, lines 62-64.

At the time of the invention, it would have been obvious to someone of ordinary skill in the art, given these references, to combine the above packet buffering and processing teachings of *Robotham* with the above fragmentation and reassembly teachings of *Bilic* in view of *Malagrino* in order to provide an efficient method of buffering

and processing reassembled packets for onward transmission as spoken of on column 3, lines 56-58 of *Robotham*.

Robotham does not teach that “responsive to non-existence of the connection table entry, sending the first packet to network interface software for preparing the first packet for the network interface circuitry, the network interface software for generating an address resolution table (ART) index for an address resolution table entry that stores a media access control (MAC) address and MAC layer attributes” and “building the connection table entry, including the ART index”.

However, *Natanson* teaches a method of MAC address learning, where a hash table 76 is created, and where new entries are added (responsive to non-existence of entry) by adding the new MAC source address that functions as an index to a corresponding LEC_ID as spoken of on column 15, lines 46-54.

Natanson also teaches how two tables, an LE_ARP table having MAC (index) to ATM address mappings, and an LEC_ID table, having ATM address (index) to LEC_ID mappings, are used in conjunction to retrieve a particular LEC_ID corresponding to a MAC address (index) as spoken of on column 15, lines 55-60.

At the time of the invention, it would have been obvious to someone of ordinary skill in the art, given these references, to combine the MAC address index teachings of *Natanson* with the context table teachings of *Robotham* in order to allow for the efficient processing of new flows of packets (using fragmentation and reassembly as taught in *Bilic in view of Malagrino*) originating from end users using MAC enabled (e.g. Ethernet, 802.11) devices.

Regarding claims **6, 15, and 26**, *Bilic* further teaches UDP/IP packet processing as spoken of on column 7, lines 7-11.

Regarding claims **7, 14, and 27,** *Robotham* further teaches that the count values (total count signal) in the count table 40 are adjusted to always reflect the current state (whether packets have been partially processed) of the buffer 20 as spoken of on column 3, lines 62-66.

At the time of the invention, it would have been obvious to someone of ordinary skill in the art, given these references, to combine the above packet buffering and processing teachings of *Robotham* with the above fragmentation and reassembly teachings of *Bilic* in view of *Malagrino* in order to provide an efficient method of buffering and processing reassembled packets for onward transmission as spoken of on column 3, lines 56-58 of *Robotham*.

Regarding claims **8 and 16,** *Robotham* further teaches transmission block 50 that utilizes the stream identifier (do not use flag) to retrieve the set of independent group identifiers corresponding to the particular stream from the context table 30 as spoken of on column 3, lines 50-53.

At the time of the invention, it would have been obvious to someone of ordinary skill in the art, given these references, to combine the above packet buffering and processing teachings of *Robotham* with the above fragmentation and reassembly teachings of *Bilic* in view of *Malagrino* in order to provide an efficient method of buffering and processing reassembled packets for onward transmission as spoken of on column 3, lines 56-58 of *Robotham*.

Regarding claims **9, 10, and 17**, *Robotham* further teaches transmission block 50 (having network interface software) that determines stream identifiers (packet processing) corresponding to fetched data units (packets) as spoken of on column 3, lines 45-49.

At the time of the invention, it would have been obvious to someone of ordinary skill in the art, given these references, to combine the above packet buffering and processing teachings of *Robotham* with the above fragmentation and reassembly teachings of *Bilic* in view of *Malagrino* in order to provide an efficient method of buffering and processing reassembled packets for onward transmission as spoken of on column 3, lines 56-58 of *Robotham*.

Response to Arguments

6. Applicant's arguments filed 10/28/08 have been fully considered but they are not persuasive.

Regarding *amended* claims **3, 11, and 23,** Applicant argues that the assembling of received fragments into frames as taught in *Bilic* does not anticipate Applicant's claimed "method for assembling a plurality of packet fragments into a packet".

Applicant further argues that the terms “packet” and “frame” have widely accepted different meanings in the area of network routing, and that a packet is typically encapsulated into one or more frames for forwarding through a network.

However, referring to column 1, lines 51-66 of *Bilic,* it is stated that the term “frame” in the disclosure of *Bilic* corresponds to transport-layer datagrams, such as TCP

or UDP segments, as well as other upper-layer datagrams that are divided among multiple packets at the network layer.

Further, referring to Applicant's specification on pages 29-30, paragraphs 90 and 91, it is disclosed how an incoming packet 101 is checked to see whether or not it is an IP fragment of either a TCP packet or a UDP packet. From this disclosure, it appears that the term "packet" in Applicant's disclosure and claims refers to transport layer data.

Therefore, it appears that the "frames" of *Bilic* and the "packets" of Applicant's disclosure and claims both constitute transport layer datagrams. It follows that the "fragments of data frames" as taught in *Bilic* correspond to the claimed "packet fragments" of Applicant's claims. Therefore, it is held that *Bilic* teaches the above limitation in question.

Applicant further argues that *Bilic* does not teach the assembling of packet fragments into a packet for transmission.

However, as provided above, while *Bilic* teaches the reassembly of packet fragments by network interface adapter 20 and forwarding (transmission) of the reassembled packet data to a host 24 via a bus interface 40 and host bus 42, *Bilic* does not explicitly teach "transmitting the first packet from the network interface circuitry <u>over a network</u> to a receiver".

However, *Malagrino* teaches a system and method for efficient reassembly of fragments, where upon a switch S5 receiving fragments 212 of a packet, switch S5 reassembles the fragments into packet 210 and subsequently forwards the packet 210

over network 230 to host H2 (receiver) as shown in Figure 2 and spoken of on column 6, lines 1-11.

At the time of the invention, it would have been obvious to someone of ordinary skill in the art, given these references, to apply the above reassembled packet transmission teachings of *Malagrino* to the teachings of *Bilic* in order to provide support for packet forwarding to hosts that are located remotely (rather than local to) from the packet fragment reassembly processor as spoken of on column 6, lines 1-11 of *Malagrino*.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL J. MOORE, JR., whose telephone number is (571)272-3168. The examiner can normally be reached on Monday-Friday (7:30am - 4:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jayanti K. Patel can be reached at (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Michael J. Moore, Jr./
Examiner, Art Unit 2419